AMENDMENTS TO THE CLAIMS

1. (Currently amended) A package (38) for encasing at least one semiconductor device (28), comprising:

a lead frame including an electrically conductive substrate and having opposing first and second sides,

said first side of said lead frame having a planar first side surface and an array of lands (14), each of said lands protruding from said first side surface, said lands adapted to be bonded to external circuitry and being arranged in a first pattern, and

said second side of said lead frame having a planar second side surface and an array of chip attach sites (24), each of said chip attach sites protruding from said second side surface, said chip attach sites being arranged in a second pattern and being directly electrically interconnected by interconnections (30) to input/output pads on said at least one semiconductor device (28), said chip attach sites disposed opposite said input/output pads, and

a plurality of electrically isolated routing circuits (26) electrically interconnecting individual combinations of said array of lands (14) and said array of chip attach sites (24);

a first molding compound (18) disposed on said first side surface and between individual lands of said array of lands (14); and

a second molding compound (36) encapsulating said at least one semiconductor device (28), said array of chip attach sites (24) and said routing circuits (26),

wherein

the lands and chip attach sites are formed from ~~integral with the substrate in~~ a monolithic electrically conductive structure, and

the array of lands has a larger lateral extent than the array of chip attach sites.

2. (Previously presented) The package (38) of claim 1 wherein said lead frame and said routing circuits (26) are elements of a single electrically conductive substrate (10).

3. (Previously presented) The package (38) of claim 2 wherein said single electrically conductive substrate (10) is copper or a copper-base alloy.

4. (Original) The package (38) of claim 2 wherein a first perimeter defined by said array of lands (14) does not exceed a second perimeter defined by said at least one semiconductor device (28).

5. (Original) The package (38) of claim 4 being a chip scale package.

6. (Original) The package (38) of claim 2 wherein a distance (32) between said at least one semiconductor device (28) and said routing circuits (26) is at least 75 microns and a space defined by said distance (32) is filled with said second molding compound (36).

7. (Original) The package (38) of claim 6 wherein said distance (32) is from 100 microns to 150 microns.

8. (Previously presented) The package (38) of claim 2 further including a heat sink (42) that is a single electrically conductive substrate with said lead frame and coplanar with said array of lands (14).

9. (Previously presented) The package (38) of claim 2 further including a die pad (44) for bonding one of said at least one semiconductor devices (28), said die pad (44) being monolithic with said lead frame.

10. (Previously presented) The package (38) of claim 2 further including bond sites for bonding a passive device (52), said bond sites being monolithic with said lead frame.

11. (Original) The package (38) of claim 2 wherein said array of lands (14) and said first molding compound (18) are coplanar.

12. (Original) The package (38) of claim 2 wherein said array of lands (14) extend beyond said first molding compound (18).

13-20. (Cancelled)

21. (Previously presented) The package (38) of claim 1 wherein the chip attach sites (24) are not coplanar with the routing circuits (26).

22. (Previously presented) The package (38) of claim 2 wherein a distance (32) between said at least one semiconductor device (28) and said routing circuits (26) is at least 25 microns and a space defined by said distance (32) is filled with said second molding compound (36).